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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,189	KRISHNAN, SIVARAM	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,10-12,14,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,10-12,14,15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 15 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Response mailed on September 29, 2005. Claim 1 was amended. Claims 1-3, 5-6, 10-12, 14-15 and 17-18 of the application are pending. This office action is made non-final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3, 5-6, 10-12, 14-15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mizuno et al.** (U.S. Patent 6,370,494) in view of **Hellestrand et al.** (U.S. Patent 6,230,114).

4.1 **Mizuno et al.** teaches Simulator ... for execution on computer realizing the simulator... Specifically, as per Claim 10, **Mizuno et al.** teaches a simulation system for simulating the performance of an external system (Fig. 1;CL1, L9-12); the simulation system comprising:

a module for performing simulation in a first simulation mode for at least a first portion of code that models at least a portion of the external system (Fig. 1, Item 11; Fig. 3; CL1, L38-62; CL2, L9-14; CL4, L19-27); and

a module for performing simulation in a second simulation mode for at least a second portion of code that models at least a portion of the external system (Fig 1, Item 12; Fig 3; CL1, L38-62; CL2, L9-14; CL4, L19-27).

Mizuno et al. does not expressly teach first simulation mode having a first accuracy level. **Hellestrand et al.** teaches first simulation mode having a first accuracy level (CL4, L26-34; CL35, L18-26; CL35, L27-34), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when faster execution time is required a simpler model will be used such as simulating the processor operation without pipeline effects (CL35, L18-20) and calculating timing using time delays determined during the analysis of the user program (CL35, L31-34). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that

included first simulation mode having a first accuracy level. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when faster execution time was required a simpler model would be used such as simulating the processor operation without pipeline effects) and calculating timing using time delays determined during the analysis of the user program.

Mizuno et al. does not expressly teach second simulation mode having a second accuracy level different from the first accuracy level. **Hellestrand et al.** teaches second simulation mode having a second accuracy level different from the first accuracy level (CL4, L26-34; CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when higher timing accuracy is required an accurate timing model will be used (CL36, L22-25; CL35, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included second simulation mode having a second accuracy level different from the first accuracy level. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when higher timing accuracy is required an accurate timing model would be used.

4.2 As per Claim 11, **Mizuno et al.** and **Hellestrand et al.** teach the system of claim 10. **Mizuno et al.** teaches the first simulation mode comprises a functional simulation mode in which behavior of the external system represented by the first portion of code is simulated

without regard to execution time to thereby obtain information about functionality of the first portion of the simulated external system (CL1, L9-12; CL1, L24-28).

Mizuno et al. does not expressly teach that the second simulation mode comprises a performance simulation mode in which behavior of the external system represented by the second portion of code is simulated with regard to execution time to thereby obtain information about the performance of the second portion of the simulated external system. **Hellestrand et al.** teaches that the second simulation mode comprises a performance simulation mode in which behavior of the external system represented by the second portion of code is simulated with regard to execution time to thereby obtain information about the performance of the second portion of the simulated external system (Abstract, L4-9; CL4, L63 to CL5, L3; CL5, L21-37; CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because that allows determining instruction timing and pipeline effects on the program execution timing (CL5, L2-3; CL5, L32-33). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included the second simulation mode comprising a performance simulation mode in which behavior of the external system represented by the second portion of code was simulated with regard to execution time to thereby obtain information about the performance of the second portion of the simulated external system. The artisan would have been motivated because that would allow determining instruction timing and pipeline effects on the program execution timing.

4.3 As per Claim 12, **Mizuno et al.** and **Hellestrand et al.** teach the system of claim 10. **Mizuno et al.** teaches that the different modes are invoked within a single simulation program execution run (Fig. 2; Fig. 12; CL2, L35-38; CL3, L35-44; Cl4, L19-27).

4.4 As per Claim 14, **Mizuno et al.** and **Hellestrand et al.** teach the system of claim 11. **Mizuno et al.** does not expressly teach a module for facilitating adjustment of the second accuracy of the second performance simulation mode. **Hellestrand et al.** teaches a module for facilitating adjustment of the second accuracy of the second performance simulation mode (CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when higher timing accuracy is required an accurate timing model will be used (CL36, L22-25; CL35, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included a module for facilitating adjustment of the second accuracy of the second performance simulation mode. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when higher timing accuracy is required an accurate timing model would be used.

4.5 As per Claim 15, **Mizuno et al.** and **Hellestrand et al.** teach the system of claim 11. **Mizuno et al.** does not expressly teach that the second portion of code includes two portions of code and the system further comprises a module for facilitating the adjustment of the second accuracy of the performance simulation mode for the two portions of code independently of each

other. **Hellestrand et al.** teaches that the second portion of code includes two portions of code and the system further comprises a module for facilitating the adjustment of the second accuracy of the performance simulation mode for the two portions of code independently of each other (CL4, L26-34; CL35, L18-26; CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when higher timing accuracy is required an accurate timing model will be used (CL36, L22-25; CL35, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included the second portion of code including two portions of code and the system further comprising a module for facilitating the adjustment of the second accuracy of the performance simulation mode for the two portions of code independently of each other. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when higher timing accuracy is required an accurate timing model would be used.

4.6 As per Claim 18, **Mizuno et al.** and **Hellestrand et al.** teach the system of claim 10. **Mizuno et al.** teaches that all of the system to be simulated is modeled using computer code (Fig. 1, Item 1; Fig. 2; CL3, L36 to CL4, L31);

the module for performing simulation in a first simulation mode performs a functional simulation on all of the external system (Fig. 1, Item 11; Fig. 2, Items s11 and S21; CL4, L1-7);

the module for performing simulation in a second simulation mode performs simulation of at least a part of the external system (Fig. 1, Item 12; Fig. 2, Item 22; CL2, L52-55); and

the modules for performing the first simulation mode and the second simulation mode are invoked during a single simulation program execution run (Fig. 2; Fig. 12; CL2, L35-38; CL3, L35-44; Cl4, L19-27).

4.7 As per Claim 1, **Mizuno et al.** teaches a method of simulating a system (Fig. 1;CL1, L9-12); the method comprising:

modeling the system to be simulated using computer code to produce a system model comprising at least a first portion and a second portion (CL2, L9-14; CL2, L35-38; CL23, L61 to CL3, L4; CL3, L10-15);

in a simulator, performing simulation in a first simulation mode for at least a first portion of code comprising the first portion of the system model (Fig. 1, Item 11; Fig. 3; CL1, L38-62; CL2, L9-14; CL4, L19-27); and

in the same simulator performing simulation in a second simulation mode for at least a second portion of code comprising the second portion of the system model (Fig 1, Item 12; Fig 3; CL1, L38-62; CL2, L9-14; CL4, L19-27).

Mizuno et al. does not expressly teach first simulation mode having a first accuracy level. **Hellestrand et al.** teaches first simulation mode having a first accuracy level (CL4, L26-34; CL35, L18-26; CL35, L27-34), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when faster execution time is required a simpler model will be used such as simulating the processor operation without pipeline effects (CL35, L18-20) and calculating timing using time delays determined during the analysis of the user program (CL35,

L31-34). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included first simulation mode having a first accuracy level. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when faster execution time was required a simpler model would be used such as simulating the processor operation without pipeline effects) and calculating timing using time delays determined during the analysis of the user program.

Mizuno et al. does not expressly teach second simulation mode having a second accuracy level different from the first accuracy level. **Hellestrand et al.** teaches second simulation mode having a second accuracy level different from the first accuracy level (CL4, L26-34; CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when higher timing accuracy is required an accurate timing model will be used (CL36, L22-25; CL35, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Mizuno et al.** with the system of **Hellestrand et al.** that included second simulation mode having a second accuracy level different from the first accuracy level. The artisan would have been motivated because the speed of execution would depend on the accuracy level of the model; and when higher timing accuracy is required an accurate timing model would be used.

4.8 As per Claims 2, 3, 5, 6 and 17, these are method claims reciting the same limitations as Claims 11, 12, 14, 15 and 18. Therefore, Claims 2, 3, 5, 6 and 17 are rejected based on the same

reasoning as Claims 11, 12, 14, 15 and 18, supra, as taught throughout by **Mizuno et al.** and **Hellestrand et al.**

Response to Arguments

5. As per the Applicant's argument that "Mizuno et al. do not show a first accuracy level and a second accuracy level when they run a simulation; Hellestrand et al. show using a hardware simulator; "thus where a greater timing accuracy is required or desired than provided by running the user program completely on the host computer system, those aspects of the target processor's execution where greater accuracy is required may be modeled in hardware; such hardware is then included in the digital circuitry simulated by the hardware simulator; Hellestrand et al. however, do not show simulation occurs at a second accuracy level different from the first accuracy level for at least a second portion of code comprising the second portion of the system model", the Examiner respectfully disagrees.

Hellestrand teaches that when modeling **one or more aspects of the target processor's execution** in hardware using **the hardware simulator**, a user may select the **level of modeling accuracy** (CL35, L27-30). The Examiner takes the position that the **hardware simulator is a software model** of the hardware typically **written in the HDL**. This is the **full software approach**. Hellestrand states that as an alternative, where greater accuracy is required than provided by running the user program completely on the host computer system, **those aspects of**

the target processor's execution where greater accuracy is required may be modeled in hardware. This is the **partial hardware approach**.

Hellestrand et al. teaches in a simulator, performing simulation in a first simulation mode having a first accuracy level for at least a first portion of code comprising the first portion of the system model (CL4, L26-34; CL35, L18-26; CL35, L27-34), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when faster execution time is required a simpler model will be used such as simulating the processor operation without pipeline effects (CL35, L18-20) and calculating timing using time delays determined during the analysis of the user program (CL35, L31-34). **Hellestrand et al.** teaches in the same simulator performing simulation in a second simulation mode having a second accuracy level different from the first accuracy level for at least a second portion of code comprising the second portion of the system model (CL4, L26-34; CL35, L27-45; CL35, L63 to CL36, L12; CL36, L19-29), because the speed of execution depends on the accuracy level of the model (CL36, L13-18); and when higher timing accuracy is required an accurate timing model will be used (CL36, L22-25; CL35, L35-40).

Hellestrand provides for different levels of accuracy within the full software approach to simulation. In addition, when higher accuracy is required, he provides for partial hardware implementation of the simulator.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
November 10, 2005